• General Description

It combines trench MOSFET technology with a low resistance package to provide extremely low $R_{DS(ON)}$.

• Features

■Low $R_{DS(ON)}$ to minimize conductive loss

■Low Gate Charge for fast switching

■Low Thermal resistance

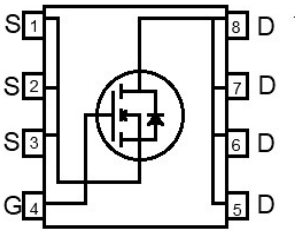
•Application

■BLDC Motor driver

■DC-DC

■Battery protection

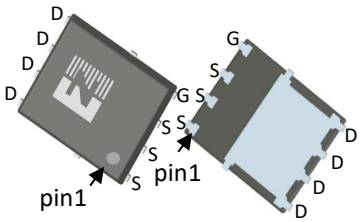
• Product Summary



V_{DS}= 30V

$R_{DS(ON)}$ = 2.5mΩ

I_D= 95A



DFN5*6

RoHS

REACH COMPLIANT

HF

•Ordering Information:

Part NO.	ZMS023N03NA
Marking	ZMS023N03N
Packing Information	REEL TAPE
Basic ordering unit (pcs)	3000

•Absolute Maximum Ratings (T_C=25℃)

Parameter	Symbol	Conditions	Value	Unit
Drain-Source Voltage	V_{DS}		30	V
Gate-Source Voltage	V_{GS}		±20	V
Continuous Drain Current	I_D	T_C=25℃	95	A
	I_D	T_C=75℃	79	A
	I_D	T_C=100℃	64	A
Pulsed Drain Current	I_{DM}	Pulsed; t_p ≤ 10 μs; T_{mb} = 25 °C;	380	A
Total Power Dissipation	P_D	T_C=25℃	63	W
Total Power Dissipation	P_D	T_A=25℃	2.8	W
Operating Junction Temperature	T_J		-55 to +150	℃
Storage Temperature	T_{STG}		-55 to +150	℃
Single Pulse Avalanche Energy	E_{AS}	L=0.1mH, V_{GS}=10V, Rg=25Ω,	110	mJ
		L=0.5mH, V_{GS}=10V, Rg=25Ω,	231	mJ
ESD Level (HBM)	CLASS 2			

•Thermal resistance

Parameter	Symbol	Min.	Typ.	Max.	Unit
Thermal resistance, junction - case	R_{thJC}		-	2	°C/W
Thermal resistance, junction-ambient①	R_{thJA}		-	45	°C/W
Soldering temperature	Tsold		-	260	°C

•Electronic Characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} =0V, I_D =250uA	30			V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} =V_{DS}, I_D =250uA	1.3	1.8	2.5	V
Drain-Source Leakage Current	I_{DSS}	V_{GS}=0V, V_{DS}= 30V			1.0	uA
Gate- Source Leakage Current	I_{GSS}	V_{GS}=±20V, V_{DS} = 0V			100	nA
Static Drain-source On Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D= 24A		2.5	3.0	mΩ
		V_{GS}=4.5V, I_D= 12A		3.4	4.3	mΩ
Forward Transconductance	g_{FS}	V_{DS} =5V, I_{SD} = 10A		20		s
Diode Forward Voltage	V_{FSD}	V_{GS} =0V, I_{SD} = 24A			1.3	V

•Dynamic characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input capacitance	Ciss	f = 1MHz, V_{DS}=25V	-	1997	-	pF
Output capacitance	Coss		-	558	-	
Reverse transfer capacitance	Crss		-	43	-	
Gate Risistance	Rg	f = 1MHz	-	1		Ω
Total gate charge	Qg	V_{DD} = 15V, I_D = 24A, V_{GS} = 10V	-	32	-	nC
	Qg (4.5v)		-	14	-	
Gate - Source charge	Qgs		-	5.7	-	
Gate - Drain charge	Qgd		-	6	-	
Turn-ON Delay time	$t_{D(on)}$	V_{GS}=10V,V_{DS}=15V, R_G =3.3Ω, I_D =20A	-	5.4	-	ns
Turn-ON Rise time	t_r		-	7	-	ns
Turn-Off Delay time	$t_{D(off)}$		-	30	-	ns
Turn-Off Fall time	t_f		-	9	-	ns
Reverse Recovery Time	t_{RR}	V_{DD}=20V, dI_S/dt = 100A/us, I_S=20A	-	22	-	ns
Reverse Recovery Charge	Q_{RR}		-	7	-	nC

Fig.1 Gate-Charge Characteristics

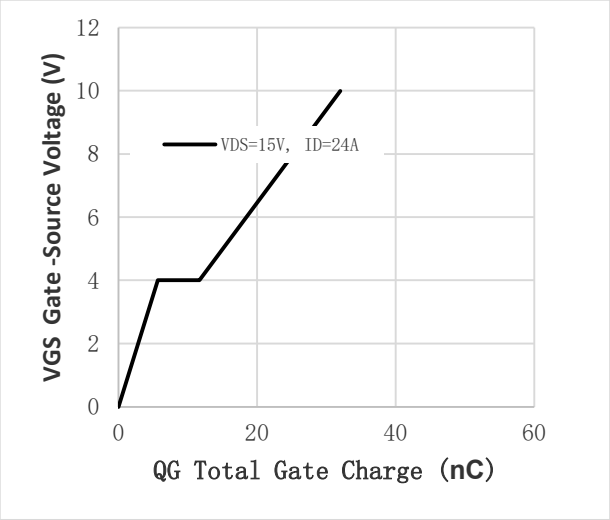


Fig.2 Capacitance Characteristics

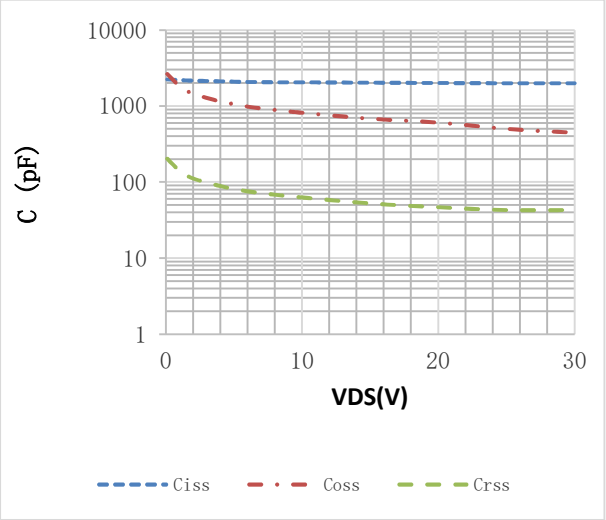


Fig.3 Power Dissipation

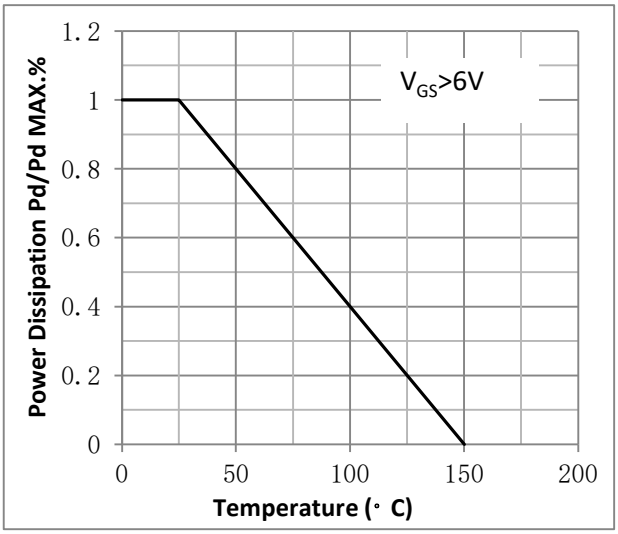


Fig.4 Typical output Characteristics

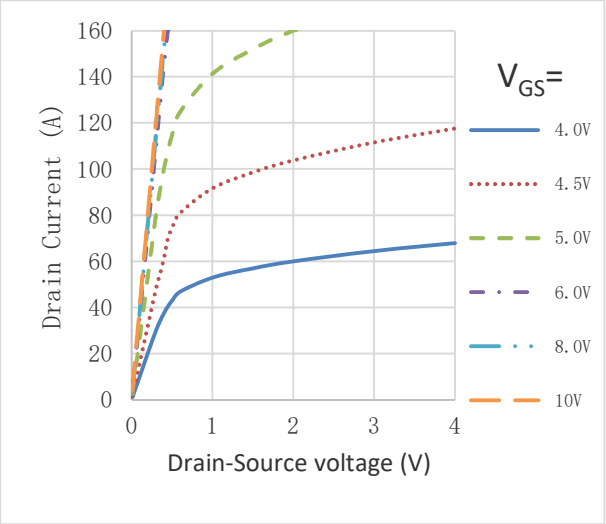


Fig.5 Threshold Voltage V.S Junction Temperature

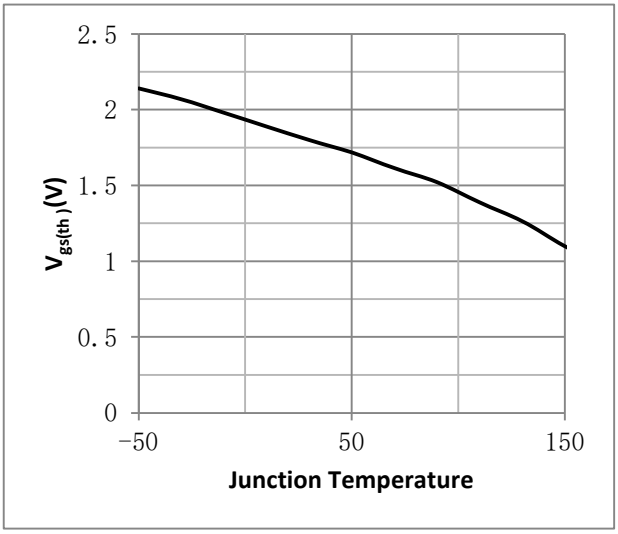


Fig.6 Resistance V.S Drain Current

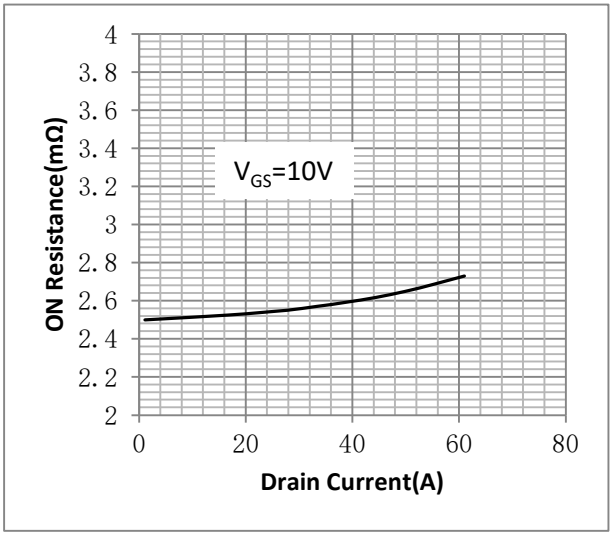


Fig.7 On-Resistance VS Gate Source Voltage

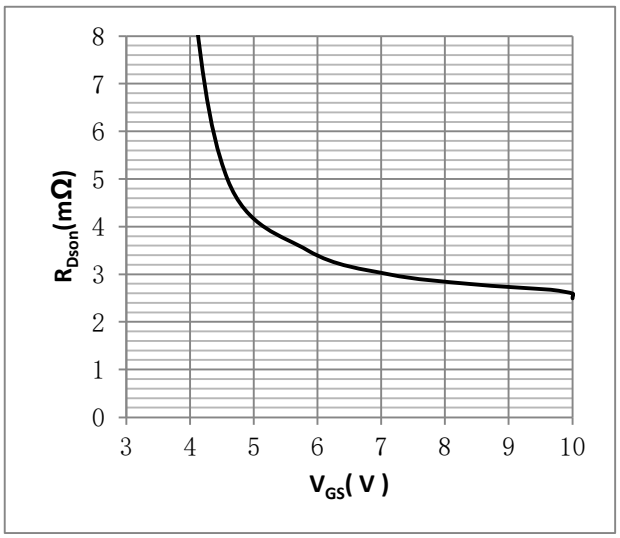


Fig.8 On-Resistance V.S Junction Temperature

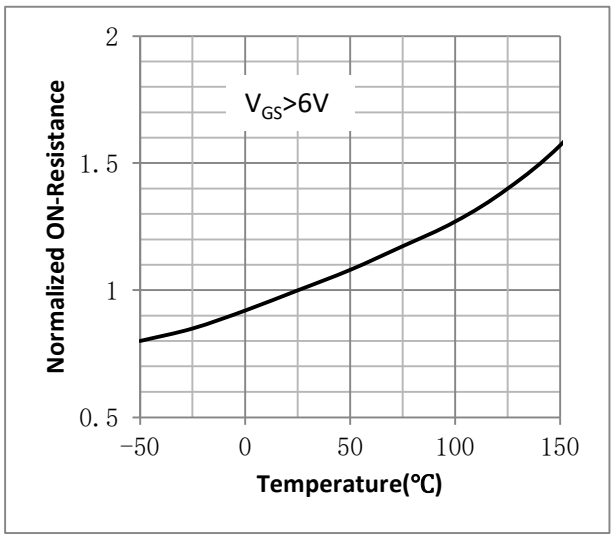


Figure 9. Diode Forward Voltage vs. Current

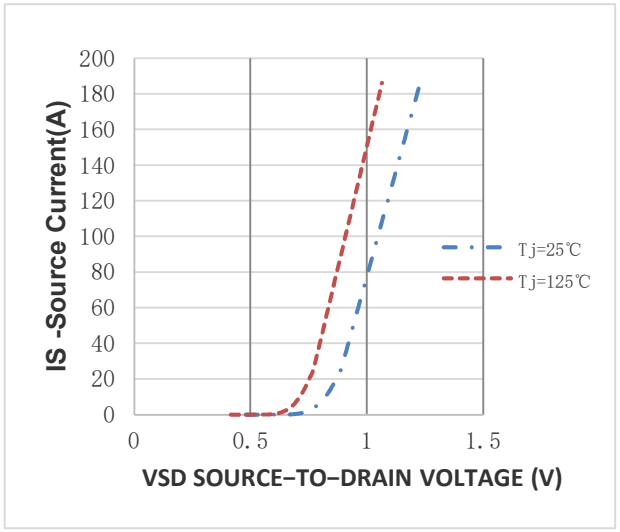


Figure 10. Transfer Characteristics

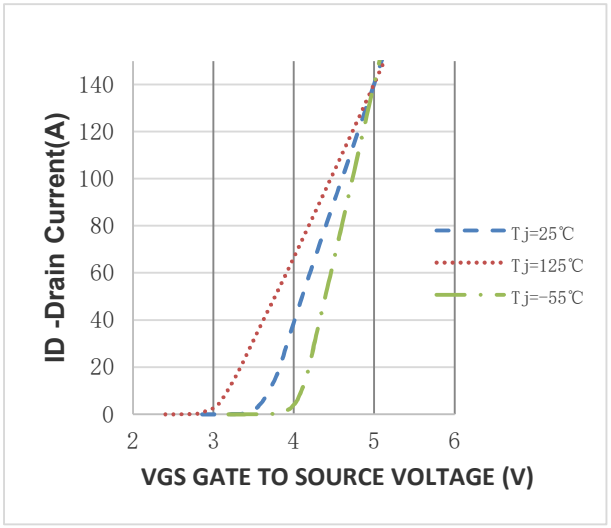


Fig.11 Safe Operating Area

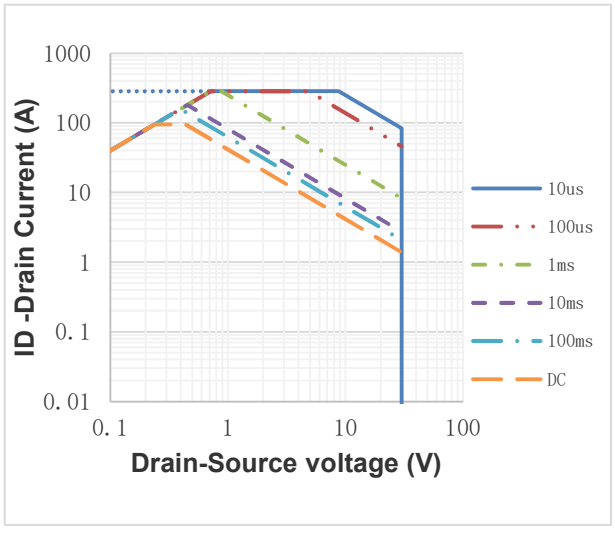


Fig.12 ID vs. Case Temperature②

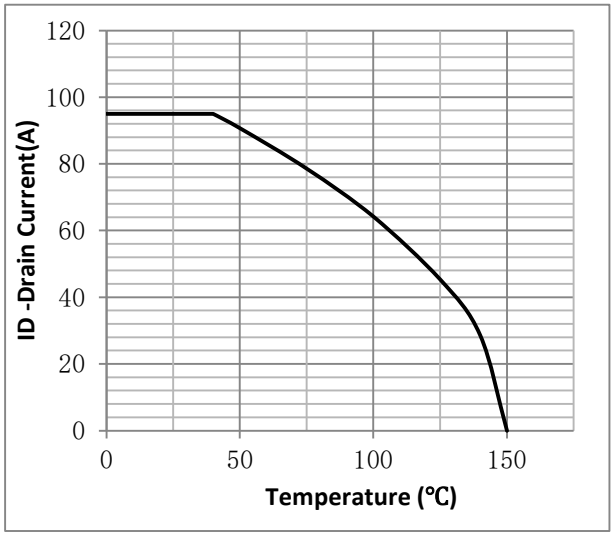
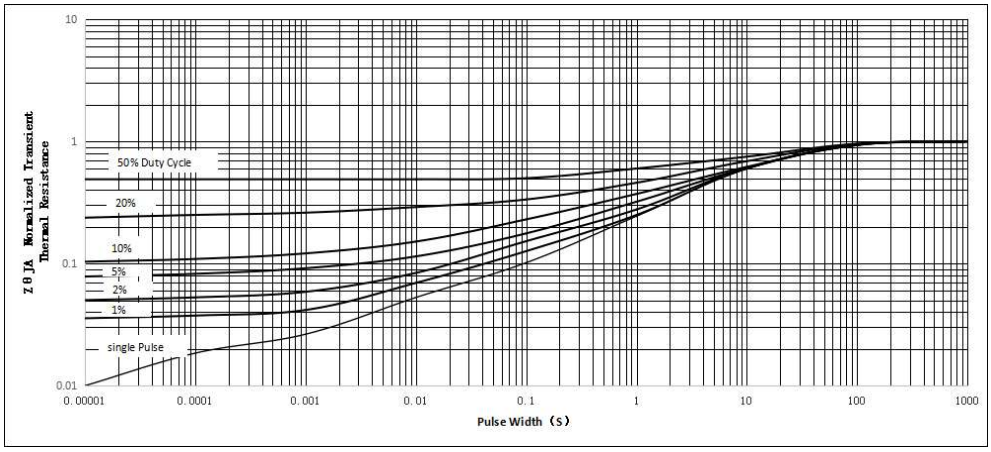
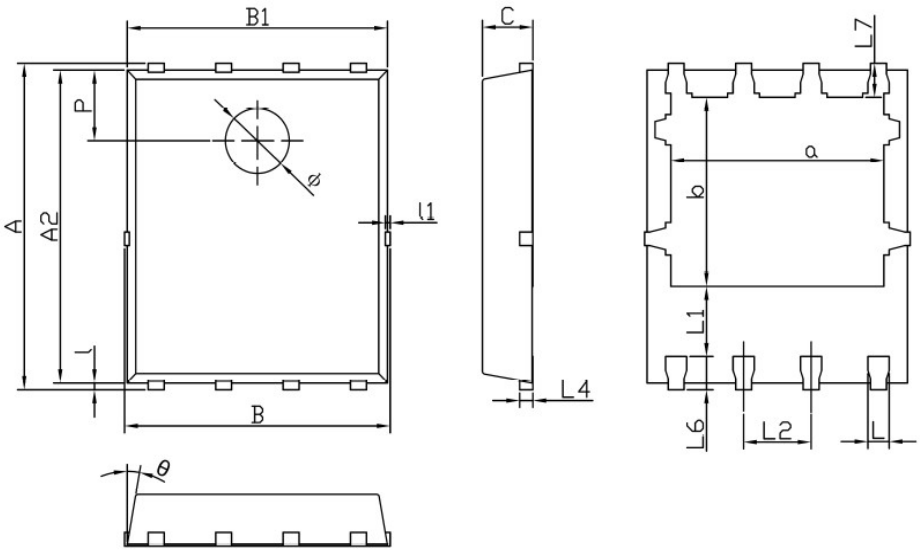


Fig.13 Normalized Maximum Transient Thermal Impedance



●DFN5*6 Package Outline



Dimensions In Millimeters			
Symbol	MIN	TYP	MAX
A	5.90	6.00	6.10
a	3.91	4.01	4.11
A2	5.70	5.75	5.80
B	4.90	5.00	5.10
b	3.375	3.475	3.575
B1	4.80	4.90	5.00
C	0.90	0.95	1.00
L	0.30	0.40	0.50
l	0.06	0.13	0.20
L1	1.10	-	-
l1	-	-	0.10
L2	1.17	1.27	1.37
L4	0.21	0.26	0.34
L6	0.51	0.61	0.71
L7	0.51	0.61	0.71
P	1.15	1.30	1.45
θ	8°	10°	12°
ϕ	1.10	1.20	1.30

Note:

① Device mounted on FR-4 substrate PC board, 2oz copper, with thermal bias to bottom layer 1inch square copper plate；

②Practically the current will be limited by PCB, thermal design and operating temperature. V_{GS}=10V.

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Revision History

Version	Date	Change
A	2025/4/2	Initial Release
B	2026/6/11	Update marking information.